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EXAMINER	
NGUYEN, STEVE N	
ART UNIT	**PAPER NUMBER**
2138	

DATE MAILED: 11/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/955,566	SHAH ET AL.	
	Examiner	Art Unit	
	Steve Nguyen	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,5-9,11-22,26-28,31-35 and 37-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5-9,11-22,26-28,31-35 and 37-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1, 2, 5-9, 11-22, 26-28, 31-35, and 37-39 are currently pending.

Claim Objections

2. In view of the amended claims, all objections in the prior Office Action are withdrawn.

Claim Rejections - 35 USC § 112

3. The U.S.C. 112, second paragraph rejection of claims 1, 14, and 27 has been withdrawn in view of the amended claims.

Response to Arguments

4. Applicant's arguments with respect to claims 1, 2, 5-9, 11-22, 26-28, 31-35, and 37-39 have been considered but are moot in view of the new ground(s) of rejection.

Claim Objections

5. Claims 14 and 27 objected to because of the following informalities:

Claim 14 recites a "one-hot vector", but it is unclear what a one-hot vector comprises. A one-hot vector is mentioned in the specification on page 66, paragraph 1 but the Applicant has not provided a concise definition of a one-hot vector. Based on

the context of page 66, paragraph 1, it is assumed that each element in the one-hot vector contains a bit which represents whether the corresponding path metric is a surviving path at a given point during the binary tree search, and that the minimum path metric is indicated exclusively by a single bit set in the vector concluding the binary tree search.

Claim 27 recites, "an output of each element in a the column is received". Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 1, 2, 5, 6, 11, 27, 28, 31, 32, and 37 rejected under 35 U.S.C. 103(a) as being unpatentable over Takamichi (US Pat. 6,615,388) in view of Akram et al (US Pat. 6,462,423; hereinafter referred to as Akram).

As per claim 1:

Takamichi teaches an apparatus for decoding data (Fig. 2) comprising:

- an array of storage elements having rows and columns (col. 3, lines 54-56), wherein an input of each element in a column receives data from only two sending elements of a previous column and an output of each element in the column is received by only two receiving elements in a next column (col. 3, lines 63-64), and
- wherein said inputs and outputs are logically interconnected according to an encoder polynomial for an error correction code (col. 3, lines 20-23; path memory 13 is interconnected according to a Viterbi code).

Not explicitly disclosed by Takamichi is wherein the receiving elements are physically the closest to each element in the column. Akram in an analogous art teaches that conventional wisdom encourages the shortest signal line possible in a circuit because the shorter the distance, the faster the signal arrives (col. 2, lines 44-52). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to place the receiving elements close to each other. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that doing so would have achieved a faster system as disclosed by Akram.

As per claim 2:

Takamichi teaches the apparatus as in claim 1, wherein said encoder polynomial is a Viterbi encoder polynomial (col. 3, lines 20-23; path memory 13 is interconnected according to a Viterbi code).

As per claim 5:

Takamichi teaches the apparatus as in claim 2 wherein the number of columns is equivalent to the depth of a Viterbi trellis (col. 3, lines 54-55; the number of columns corresponds to the number of stages of the Viterbi trellis).

As per claim 6:

Takamichi teaches the apparatus as in claim 5 above. Takamichi teaches a matrix of memory cells grouped into N stages (col. 3, lines 54-56). Although it is not specifically mentioned that N is 64, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to include 64 stages. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that the N stages disclosed by Takamichi could be any number of stages that were applicable to a particular Viterbi polynomial.

As per claim 11:

Takamichi teaches the apparatus as in claim 1 further comprising minimization logic to identify a storage element in a final column of said matrix from which to select data (col. 4, lines 14-18).

As per claim 27:

Takamichi teaches a machine-readable medium having code stored thereon which defines an integrated circuit (IC), said IC comprising:

- an array of storage elements having rows and columns (col. 3, lines 54-56), wherein an input of each element in a column receives data from only two sending elements of a previous column and an output of each element in the column is received by only two receiving elements in a next column (col. 3, lines 63-64), and
- wherein said inputs and outputs are logically interconnected according to an encoder polynomial for an error correction code (col. 3, lines 20-23; path memory 13 is interconnected according to a Viterbi code).

Not explicitly disclosed by Takamichi is wherein the receiving elements are physically the closest to each element in the column. Akram in an analogous art teaches that conventional wisdom encourages the shortest signal line possible in a circuit because the shorter the distance, the faster the signal arrives (col. 2, lines 44-52). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to place the receiving elements close to each other. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that doing so would have achieved a faster system as disclosed by Akram.

As per claim 28:

Takamichi further teaches a machine-readable medium as in claim 27 wherein said encoder polynomial is a Viterbi encoder polynomial (col. 3, lines 20-23; path memory 13 is interconnected according to a Viterbi code).

As per claim 31:

Takamichi further teaches a machine-readable medium as in claim 28 wherein the number of columns is equivalent to the depth of a Viterbi trellis (col. 3, lines 54-55; the number of columns corresponds to the number of stages of the Viterbi trellis).

As per claim 32:

Takamichi teaches a machine-readable medium as in claim 31 above. Takamichi teaches a matrix of memory cells grouped into N stages (col. 3, lines 54-56). Although it is not specifically mentioned that N is 64, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to include 64 stages. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that the N stages disclosed by Takamichi could be any number of stages that were applicable to a particular Viterbi polynomial.

As per claim 37:

Takamichi teaches the machine-readable medium as in claim 27 further comprising minimization logic to identify a storage element in a final column of said matrix from which to select data (col. 4, lines 14-18).

7. Claims 7-9, 12, 13, 33-35, 38, and 39 rejected under 35 U.S.C. 103(a) as being unpatentable over Takamichi in view of Akram in further view of Park (US Pat. 5,446,746).

As per claim 7:

Takamichi teaches the apparatus as in claim 1 further comprising: selection signals for selecting data for each element in the column from said sending elements of a previous column (col. 3, lines 45-47 and col. 4, lines 19-24).

Not explicitly mentioned is said selection signals generated based on a minimum path metric associated with each storage element. However, Park teaches producing select signals for a storage element based on a minimum path metric to find the maximum likelihood path (col. 4, lines 23-28). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to generate selection signals based on a minimum path metric. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have motivated to do so in order to recover erroneous data based on maximum likelihood as detailed by Takamichi in col. 4, lines 14-18.

As per claim 8:

Takamichi further teaches the apparatus as in claim 7 wherein selection signals select data for elements in each of said rows in said matrix (col. 3, lines 57-60), thereby specifying for all elements in each row which of said elements from a previous column

to select, said selections causing data to propagate through said matrix according to said encoder polynomial (col. 4, lines 7-14).

As per claim 9:

Takamichi further teaches the apparatus as in claim 8 wherein said selection signals are generated by add-compare-select units (col. 3, lines 45-53) selecting the lowest of potential path metrics (detailed above).

As per claim 12:

Takamichi teaches the apparatus as in claim 11 but does not explicitly disclose wherein said minimization logic identifies said storage element based on said storage element having a minimum path metric associated therewith.

However, Park teaches producing select signals for a storage element based on a minimum path metric to find the maximum likelihood path (col. 4, lines 23-28). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to identify a minimum path metric. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have motivated to do so in order to recover erroneous data based on maximum likelihood as detailed by Takamichi in col. 4, lines 14-18.

As per claim 13:

Park further teaches the apparatus as in claim 12 wherein said minimum path metric is determined based on a minimum of accumulator values of add-compare-select

units associated with each of said rows (col. 4, lines 34-41; the values must be stored in an accumulator or storage element).

As per claim 33:

Takamichi teaches a machine-readable medium as in claim 27 further comprising: selection signals for selecting data for each element in each column from said elements of a previous column (col. 3, lines 45-47 and col. 4, lines 19-24).

Not explicitly mentioned is said selection signals generated based on a minimum path metric associated with each storage element. However, Park in an analogous art teaches producing select signals for a storage element based on a minimum path metric to find the maximum likelihood path (col. 4, lines 23-28). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to generate selection signals based on a minimum path metric. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have motivated to do so in order to recover erroneous data based on maximum likelihood as detailed by Takamichi in col. 4, lines 14-18.

As per claim 34:

Takamichi further teaches a machine-readable medium as in claim 33 wherein selection signals select data for elements in each of said rows in said matrix (col. 3, lines 57-60), thereby specifying for all elements in each row which of said elements from a previous column to select, said selections causing data to propagate through said matrix according to said encoder polynomial (col. 4, lines 7-14).

As per claim 35:

Takamichi further teaches a machine-readable medium as in claim 34 wherein said selection signals are generated by add-compare-select units (col. 3, lines 45-53) selecting the lowest of potential path metrics (detailed above).

As per claim 38:

Takamichi teaches a machine-readable medium as in claim 37 but does not explicitly disclose wherein said minimization logic identifies said storage element based on said storage element having a minimum path metric associated therewith.

However, Park teaches producing select signals for a storage element based on a minimum path metric to find the maximum likelihood path (col. 4, lines 23-28). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to identify a minimum path metric. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have motivated to do so in order to recover erroneous data based on maximum likelihood as detailed by Takamichi in col. 4, lines 14-18.

As per claim 39:

Takamichi teaches a machine-readable medium as in claim 38 above. Not explicitly disclosed by Takamichi is wherein said minimum path metric is determined based on a minimum of accumulator values of add-compare-select units associated with each of said rows. Park in an analogous art teaches determining a minimum path

metric based on accumulator values of add-compare-select circuits (col. 4, lines 34-41; the values must be stored in an accumulator or storage element).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the system of Park to find a minimum path metric. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have been motivated to do so in order to find a minimum path metric.

8. Claims 14-16 and 18-21 rejected under 35 U.S.C. 103(a) as being unpatentable over Takamichi in view of Joseph (US Pat. 6,931,424) in view of Higgins (US Pat. 5,390,198).

As per claim 14:

Takamichi teaches a forward-tracing array for decoding data comprising:

- a matrix of storage elements having rows and columns (col. 3, lines 54-56);
- connection logic for interconnecting said storage elements across columns according to an encoder polynomial such that storage elements in a column receive data from storage elements in a previous column (col. 3, lines 63-64);
- selection logic for selecting storage elements from said storage elements from which to read data based on a calculated path metric associated with each of said storage elements (col. 4, lines 14-18); and

Not explicitly disclosed by Takamichi is minimization logic to identify a storage element in a final column of said matrix from which to select data based on said storage

element having a minimum path metric associated therewith (col. 4, lines 14-18) which is found using a binary tree search to form a one-hot vector having a bit therein that corresponds to said minimum path metric.

Joseph in an analogous art teaches minimization logic using a binary tree structure for selecting a minimum path metric (Fig. 1; abstract). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the binary tree of Joseph. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that the binary tree can be used for a Viterbi algorithm for finding a minimum path metric, as disclosed by Joseph in col. 1, lines 12-20).

Also not explicitly disclosed is forming a one-hot vector having a bit therein that corresponds to said minimum path metric. Higgins in an analogous art teaches selecting a path metric and updating a memory with a bit corresponding to the path selected until a final output bit is produced that represents the minimum path metric (col. 3, lines 5-25). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to form a one-hot vector with a bit indicating the minimum path metric. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that Joseph updates each stage in Fig. 2 with a selected path until a minimum path metric is decided in the final stage, and that applying of a one-hot vector to the system of Joseph would have enabled one to monitor the minimum path in each stage.

As per claim 15:

Takamichi teaches the apparatus as in claim 14, wherein said encoder polynomial is a Viterbi encoder polynomial (col. 3, lines 20-23; path memory 13 is interconnected according to a Viterbi code).

As per claim 16:

Takamichi teaches apparatus as in claim 14 wherein said encoder polynomial includes a rate of ½ (Fig. 2).

As per claim 18:

Takamichi teaches the apparatus as in claim 15 wherein the number of columns is equivalent to the depth of a Viterbi trellis (col. 3, lines 54-55; the number of columns corresponds to the number of stages of the Viterbi trellis).

As per claim 19:

Takamichi teaches the apparatus as in claim 18 above. Takamichi teaches a matrix of memory cells grouped into N stages (col. 3, lines 54-56). Although it is not specifically mentioned that N is 64, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to include 64 stages. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that the N stages disclosed by Takamichi could be any number of stages that were applicable to a particular Viterbi polynomial.

As per claim 20:

Takamichi teaches the apparatus as in claim 14 wherein said selection logic further comprises: selection signals to select data for elements in each of said rows in said matrix, thereby specifying for all elements in each row which of said elements from a previous column to select, said selections causing data to propagate through said matrix according to said encoder polynomial (col. 3, lines 64-67 to col. 4, lines 1-14; col. 4, lines 19-24).

As per claim 21:

Takamichi teaches the apparatus as in claim 20 wherein storage elements in a first column of said matrix are loaded with constant values and said selection signals select data for elements in each of said rows (col. 3, lines 64-67 to col. 4, lines 1-6).

9. Claims 22 and 26 rejected under 35 U.S.C. 103(a) as being unpatentable over Takamichi in view of Joseph in view of Higgins as applied above, and further in view of Park.

As per claim 22:

Takamichi teaches the apparatus as in claim 21 wherein said selection signals are generated by add-compare-select units (col. 3, lines 45-53). Not explicitly disclosed is selecting the lowest of potential path metrics.

However, Park teaches producing select signals for a storage element based on a minimum path metric to find the maximum likelihood path (col. 4, lines 23-28). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to generate selection signals based on a minimum path metric.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have motivated to do so in order to recover erroneous data based on maximum likelihood as detailed by Takamichi in col. 4, lines 14-18.

As per claim 26:

Takamichi teaches the apparatus as in claim 14 above. Not explicitly disclosed by Takamichi is wherein said minimum path metric is determined based on a minimum of accumulator values of add-compare-select units associated with each of said rows. Park in an analogous art teaches determining a minimum path metric based on accumulator values of add-compare-select circuits (col. 4, lines 34-41; the values must be stored in an accumulator or storage element).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the system of Park to find a minimum path metric. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have been motivated to do so in order to find a minimum path metric.

10. Claim 17 rejected under 35 U.S.C. 103(a) as being unpatentable over Takamichi in view of Joseph in view of Higgins as applied above, and in further view of Wolf (US Pat. 5,233,630).

As per claim 17:

Takamichi teaches the apparatus as in claim 14 above. Not explicitly disclosed is wherein R=3 for an encoder polynomial rate of 1/3. However, Wolf teaches that the coding rate of ½ has become one of the most popular rates, but other rates are also generally used. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a coding rate of 1/3. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that other code rates besides ½ are used.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Japanese Patent JP 08237145 A.

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steve Nguyen whose telephone number is (571) 272-7214. The examiner can normally be reached on M-F, 9am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Steve Nguyen
Examiner
Art Unit 2138

GUY LAMARRE
PRIMARY EXAMINER